EL5152, EL5153, EL5252, EL5455

Data Sheet May 7, 2007 FN7385.5

270MHz Ultra-Accurate Amplifiers

The EL5152, EL5153, EL5252, and EL5455 are 270MHz bandwidth -3dB voltage mode feedback amplifiers with DC accuracy of <0.01%, 1mV offsets and 50kV/V open loop gains. These amplifiers are ideally suited for applications ranging from precision measurement instrumentation to high-speed video and monitor applications demanding higher linearity at higher frequency. Capable of operating with as little as 3.0mA of current from a single supply ranging from 5V to 12V dual supplies ranging from ±2.5V to ±5.0V these amplifiers are also well suited for handheld, portable and battery-powered equipment.

Single amplifiers are offered in SOT-23 packages and duals in a 10 Ld MSOP package for applications where board space is critical. Quad amplifiers are available in a 14 Ld SOIC package. Additionally, singles and duals are available in the industry-standard 8 Ld SOIC. All parts operate over the industrial temperature range of -40°C to +85°C.

Features

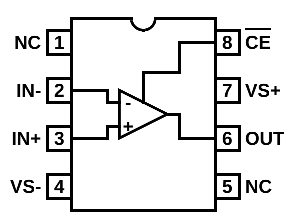
- 270MHz -3dB bandwidth
- 180V/µs slew rate
- ±1mV maximum V_{OS}
- Very high open loop gains 50kV/V
- Low supply current = 3mA
- 105mA output current
- Single supplies from 5V to 12V
- Dual supplies from ±2.5V to ±5V
- Fast disable on the EL5152 and EL5252
- Low cost
- Pb-Free plus anneal available (RoHS compliant)

Applications

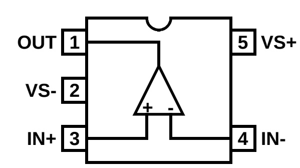
- Imaging
- Instrumentation
- Video
- Communications devices

Pinouts

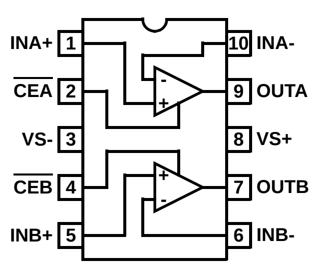
EL5152
(8 LD SOIC)
TOP VIEW



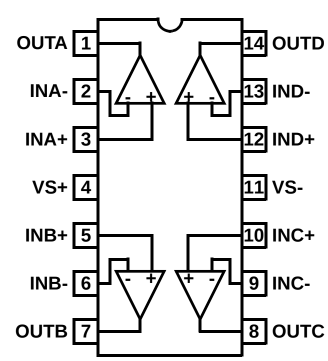
EL5153
(5 LD SOT-23)
TOP VIEW



EL5252
(10 LD MSOP)
TOP VIEW



EL5455
(14 LD SOIC)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5152IS	5152IS	-	8 Ld SOIC (150 mil)	MDP0027
EL5152IS-T7	5152IS	7”	8 Ld SOIC (150 mil)	MDP0027
EL5152IS-T13	5152IS	13”	8 Ld SOIC (150 mil)	MDP0027
EL5152ISZ (Note)	5152ISZ	-	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5152ISZ-T7 (Note)	5152ISZ	7”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5152ISZ-T13 (Note)	5152ISZ	13”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5153IW-T7	BGAA	7” (3k pcs)	5 Ld SOT-23	MDP0038
EL5153IW-T7A	BGAA	7” (250 pcs)	5 Ld SOT-23	MDP0038
EL5153IWZ-T7 (Note)	BAAL	7” (3k pcs)	5 Ld SOT-23 (Pb-free)	MDP0038
EL5153IWZ-T7A (Note)	BAAL	7” (250 pcs)	5 Ld SOT-23 (Pb-free)	MDP0038
EL5252IY	BAGAA	-	10 Ld MSOP (3.0 mm)	MDP0043
EL5252IY-T7	BAGAA	7”	10 Ld MSOP (3.0 mm)	MDP0043
EL5252IY-T13	BAGAA	13”	10 Ld MSOP (3.0 mm)	MDP0043
EL5455IS	5455IS	-	14 Ld SOIC (150 mil)	MDP0027
EL5455IS-T7	5455IS	7”	14 Ld SOIC (150 mil)	MDP0027
EL5455IS-T13	5455IS	13”	14 Ld SOIC (150 mil)	MDP0027
EL5455ISZ (Note)	5455ISZ	-	14 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5455ISZ-T7 (Note)	5455ISZ	7”	14 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5455ISZ-T13 (Note)	5455ISZ	13”	14 Ld SOIC (150 mil) (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S and GND 13.2V
Maximum Continuous Output Current 50mA
Current into I_N+, I_N-, CE 5mA
Pin Voltages . . . . GND -0.5V to V_S +0.5V

Thermal Information

Junction Temperature . . . . +125°C
Storage Temperature . . . . -65°C to +150°C
Ambient Operating Temperature . . . . -40°C to +85°C
Power Dissipation . . . . See Curves
Pb-free reflow profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = ±5V, $R_F = R_G$ = 750Ω, R_L = 150Ω, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V = +1, R_L = 500Ω, C_L = 5.0pF		270		MHz
		A_V = +2, R_L = 150Ω		85		MHz
GBWP	Gain Bandwidth Product	R_L = 150Ω		165		MHz
BW1	0.1dB Bandwidth	A_V = +1, R_L = 500Ω		50		MHz
SR	Slew Rate	V_O = -3V to +3V, A_V = +2	120	155		V/µs
		V_O = -3V to +3V, A_V = 1, R_L = 500Ω		180		V/µs
t_S	0.1% Settling Time	V_{OUT} = -1V to +1V, A_V = +2		30		ns
dG	Differential Gain Error	A_V = +2, R_L = 150Ω		0.06		%
dP	Differential Phase Error	A_V = +2, R_L = 150Ω		0.045		°
V_N	Input Referred Voltage Noise			12		nV/√Hz
I_N	Input Referred Current Noise			1.8		pA/√Hz
DC PERFORMANCE						
V_{OS}	Offset Voltage		-1	0.5	1	mV
T_CV_{OS}	Input Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		-2		µV/°C
A_{VOL}	Open Loop Gain	V_O is from -2.5V to 2.5V (EL5152 & EL5153)	10	20		kV/V
		V_O is from -2.5V to 2.5V (EL5252 & EL5455)	15	50		kV/V
INPUT CHARACTERISTICS						
CMIR	Common Mode Input Range	Guaranteed by CMRR test	-2.5		2.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 2.5 to -2.5	85	110		dB
I_B	Bias Current		-0.4	0.12	+0.6	µA
I_{OS}	Input Offset Current		-80	12	80	nA
R_{IN}	Input Resistance		25	60		MΩ
C_{IN}	Input Capacitance			1		pF
OUTPUT CHARACTERISTICS						
V_{OUT}	Output Voltage Swing	R_L = 150Ω to GND	±3.0	±3.3		V
		R_L = 500Ω to GND	±3.4	±3.7		V
I_{OUT}	Output Current	R_L = 10Ω to GND	60	105		mA
ENABLE (SELECTED PACKAGES ONLY)						
t_{EN}	Enable Time			200		ns

Electrical Specifications V_S+ = +5V, V_S- = ±5V, R_F = R_G = 750Ω, R_L = 150Ω, T_A = +25°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
t_{DIS}	Disable Time			300		ns
I_{IHCE}	$\overline{CE}$ Pin Input High Current	$\overline{CE}$ = V_S+		0	-1	µA
I_{ILCE}	$\overline{CE}$ Pin Input Low Current	$\overline{CE}$ = V_S-	5	13	25	µA
V_{IHCE}	$\overline{CE}$ Input High Voltage for Power-down		V_S+ -1			V
V_{ILCE}	$\overline{CE}$ Input Low Voltage for Power-up				V_S+ -3	V
SUPPLY						
I_{SON}	Supply Current - Enabled (per amplifier)	No load, V_{IN} = 0V, CE = +5V	2.46	3.0	3.43	mA
I_{SOFF}	Supply Current - Disabled (per amplifier)	No load, V_{IN} = 0V, $\overline{CE}$ = 5V	5	13	25	µA
PSRR	Power Supply Rejection Ratio	DC, V_S = ±3.0V to ±6.0V (EL5152 & EL5153)	85	116		dB
		DC, V_S = ±3.0V to ±6.0V (EL5252 & EL5455)	80	95		dB

Typical Performance Curves

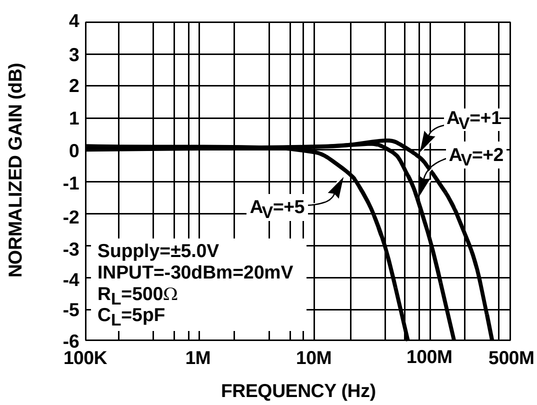


FIGURE 1. EL5152 SMALL SIGNAL FREQUENCY FOR VARIOUS GAINS

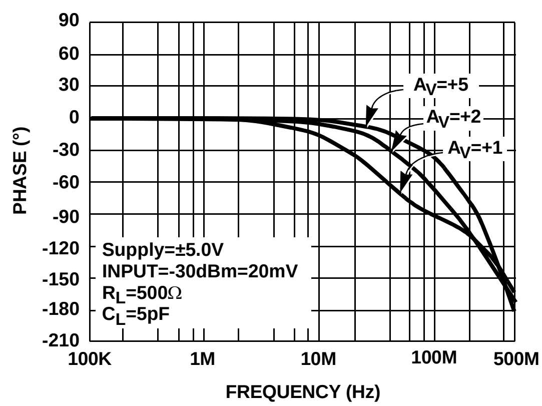


FIGURE 2. EL5152 SMALL SIGNAL FREQUENCY PHASE FOR VARIOUS GAINS

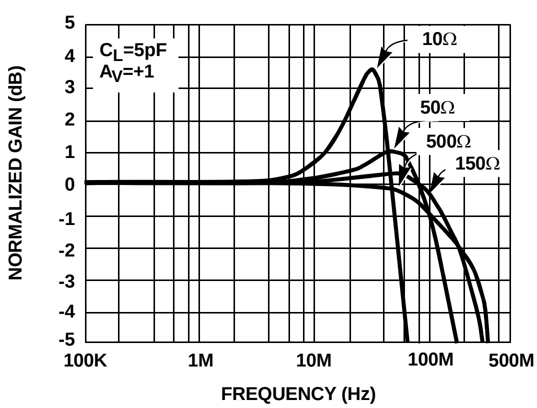


FIGURE 3. FREQUENCY RESPONSE FOR VARIOUS R_L

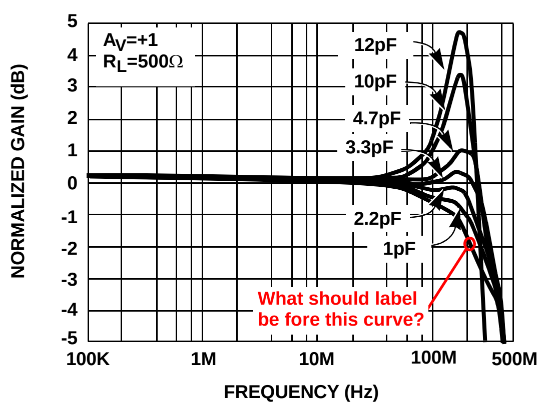


FIGURE 4. FREQUENCY RESPONSE FOR VARIOUS C_L

Typical Performance Curves (Continued)

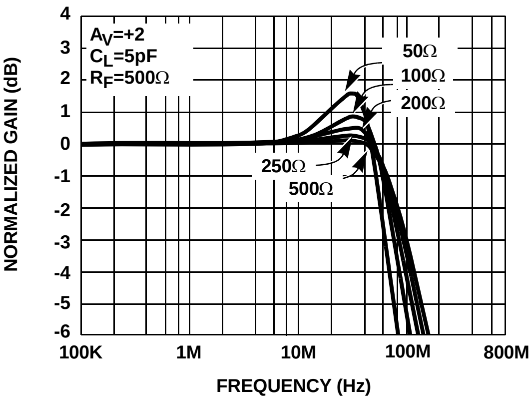


FIGURE 5. FREQUENCY RESPONSE FOR VARIOUS R_L

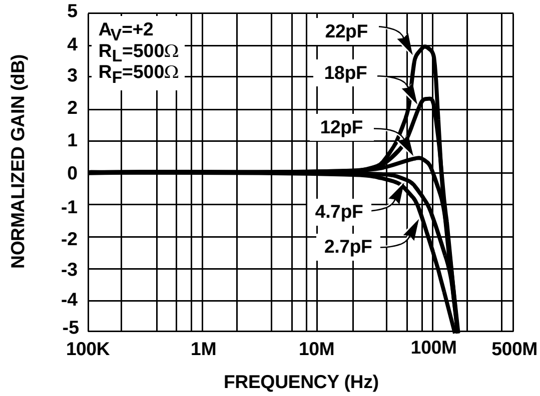


FIGURE 6. FREQUENCY RESPONSE FOR VARIOUS C_L

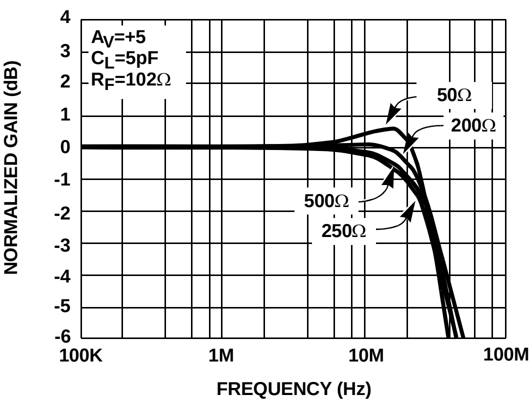


FIGURE 7. FREQUENCY RESPONSE FOR VARIOUS R_L

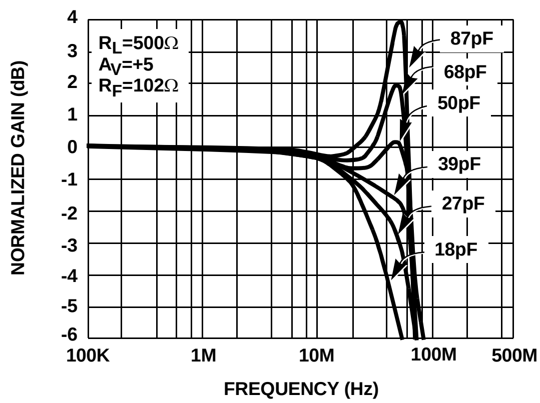


FIGURE 8. FREQUENCY RESPONSE FOR VARIOUS C_L

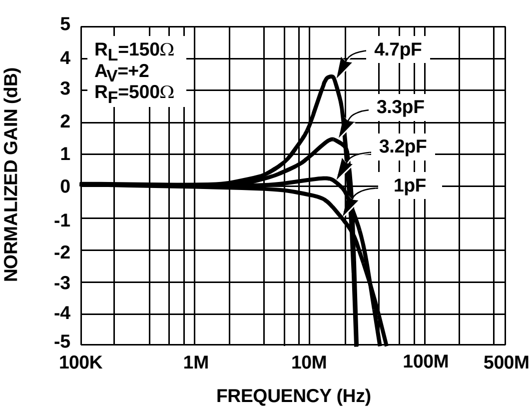


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS C_{IN}

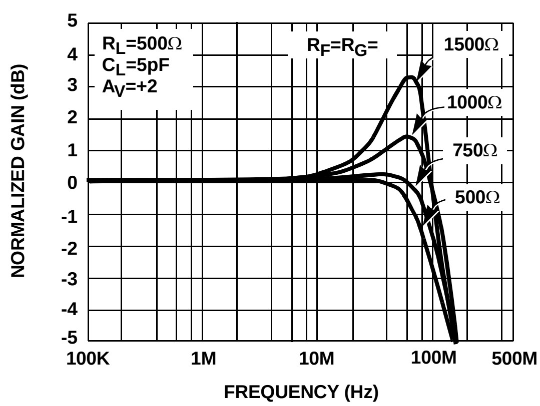


FIGURE 10. FREQUENCY RESPONSE vs R_F/R_G

Typical Performance Curves (Continued)

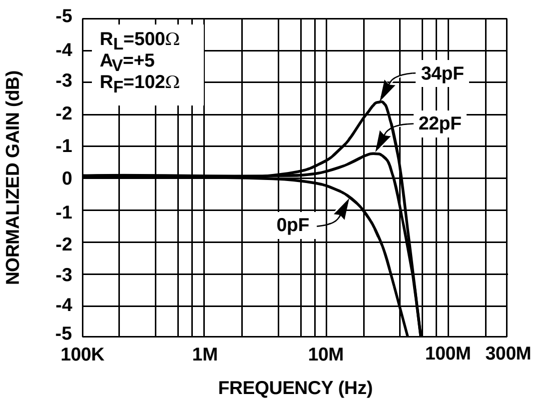


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS C_{IN}

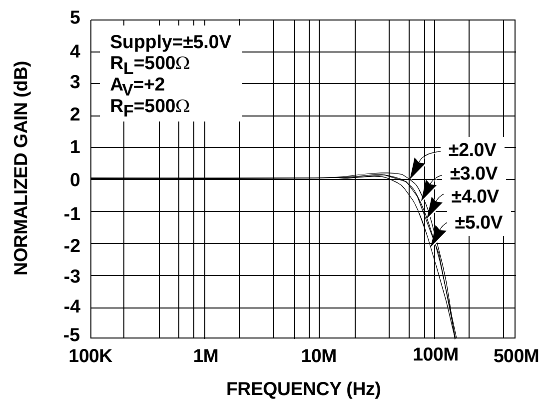


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS POWER SUPPLY

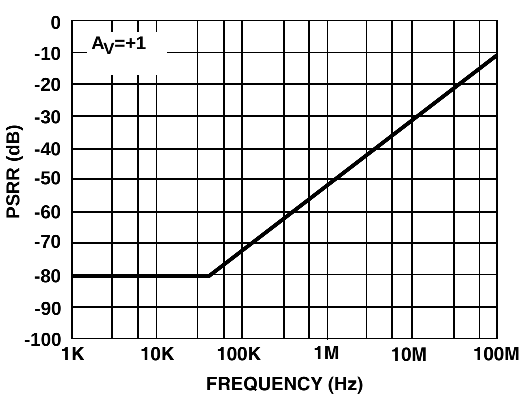


FIGURE 13. PSRR

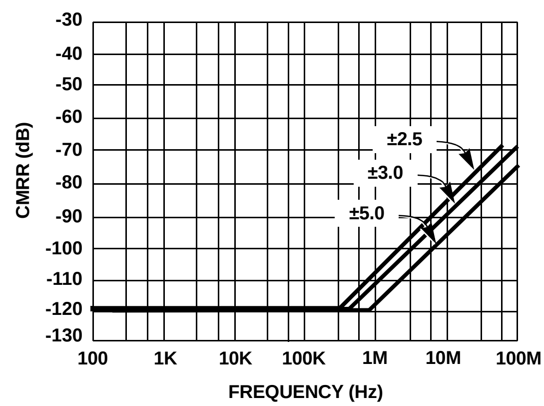


FIGURE 14. CMRR FOR VARIOUS POWER SUPPLY VALUES

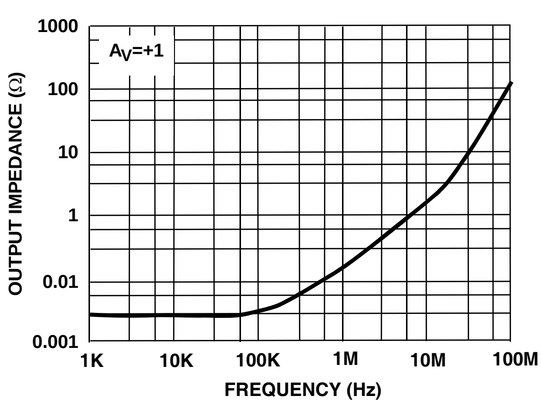


FIGURE 15. OUTPUT IMPEDANCE

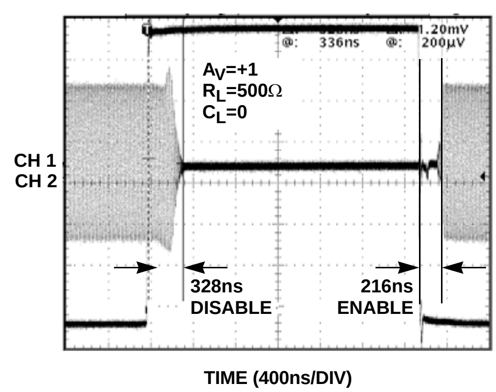


FIGURE 16. ENABLE/DISABLE RESPONSE

Typical Performance Curves (Continued)

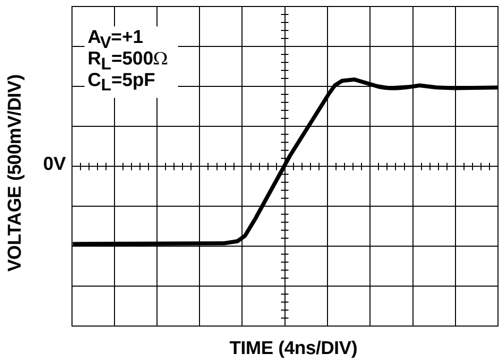


FIGURE 17. RISE TIME - LARGE SIGNAL RESPONSE

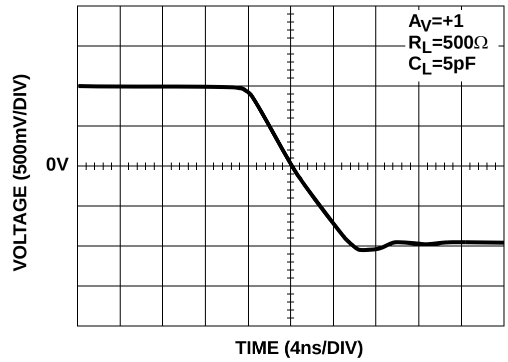


FIGURE 18. FALL TIME - LARGE SIGNAL RESPONSE

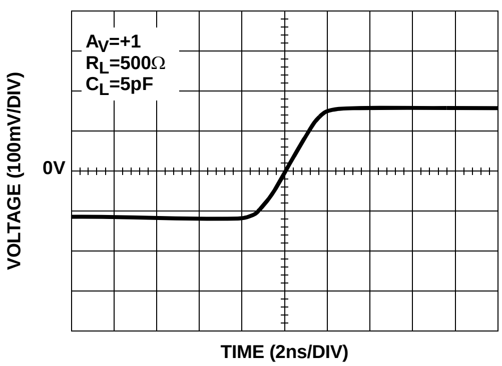


FIGURE 19. RISE TIME - SMALL SIGNAL RESPONSE

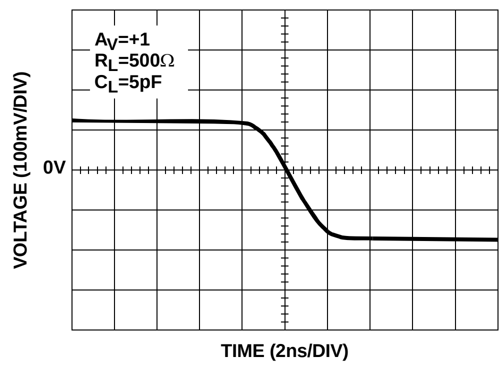


FIGURE 20. FALL TIME - SMALL SIGNAL RESPONSE

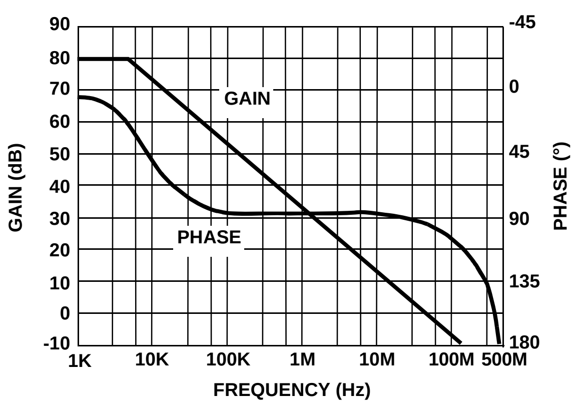


FIGURE 21. EL5152 SMALL SIGNAL OPEN LOOP GAIN vs FREQUENCY INVERTING

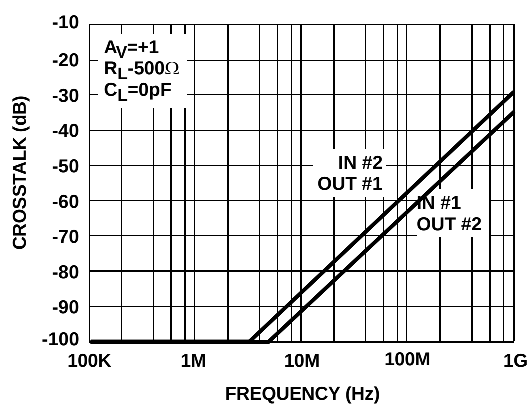


FIGURE 22. EL5252 SMALL SIGNAL FREQUENCY vs CROSSTALK

Typical Performance Curves (Continued)

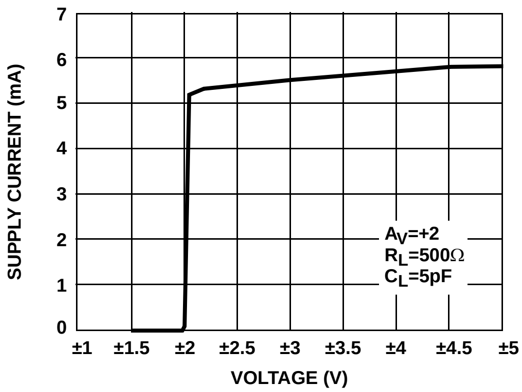


FIGURE 23. SUPPLY CURRENT vs SUPPLY VOLTAGE

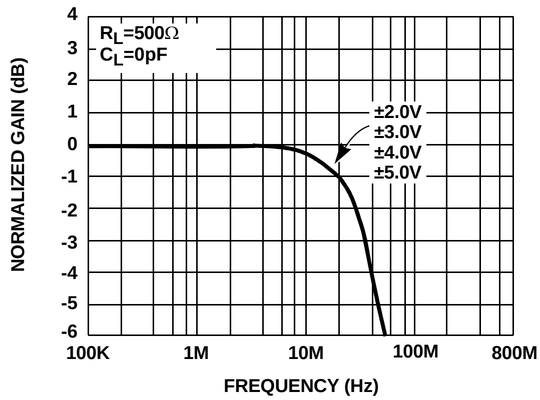


FIGURE 24. FREQUENCY RESPONSE FOR VARIOUS VOLTAGE SUPPLY LEVELS

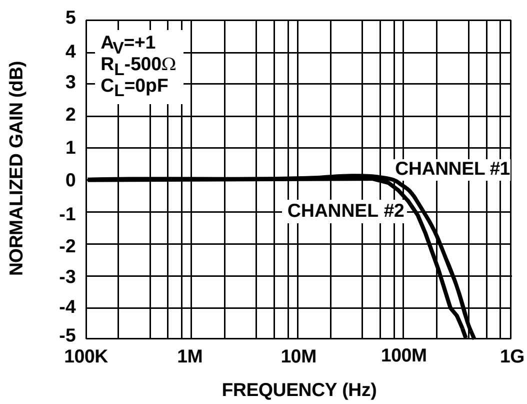


FIGURE 25. EL5252 SMALL SIGNAL FREQUENCY - CHANNEL TO CHANNEL

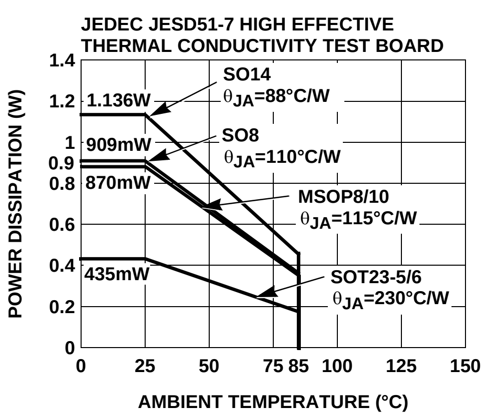


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

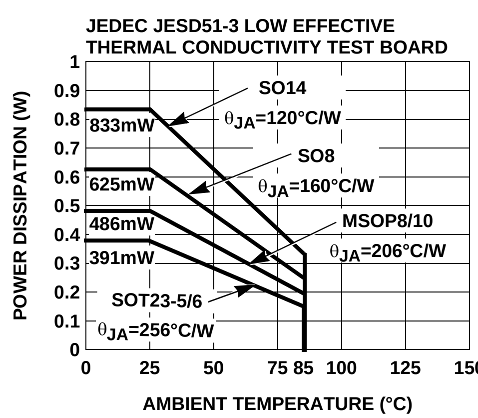


FIGURE 27. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

EL5152 Product Description

The EL5152, EL5153, EL5252, and EL5455 are wide bandwidth, low power, low offset voltage feedback operational amplifiers capable of operating from a single or dual power supplies. This family of operational amplifiers are internally compensated for closed loop gain of +1 or greater. Connected in voltage follower mode, driving a 500Ω load members of this amplifier family demonstrate a -3dB bandwidth of about 270MHz. With the loading set to accommodate typical video application, 150Ω load and gain set to +2, bandwidth reduces to about 180MHz with a 600V/µs slew rate. Power down pins on the EL5152 and EL5252 reduce the already low power demands of this amplifier family to 17µA typical while the amplifier is disabled.

Input, Output and Supply Voltage Range

The EL5152 and EL5153 families have been designed to operate with supply voltage ranging from 5V to 12V. Supply voltages range from ±2.5V to ±5V for split supply operation. Of course split supply operation can easily be achieved using single supplies by splitting off half of the single supply with a simple voltage divider as illustrated in the application circuit section.

Input Common Mode Range

These amplifiers have an input common mode voltage ranging from 1.5V above the negative supply (V_S- pin) to 1.5V below the positive supply (V_S+ pin). If the input signal is driven beyond this range the output signal will exhibit distortion.

Maximum Output Swing & Load Resistance

The outputs of the EL5152 and EL5153 families maximum output swing ranges from -4V to 4V for V_S = ±5V with a load resistance of 500Ω. Naturally, as the load resistance becomes lower, the output swing lowers accordingly; for instance, if the load resistor is 150Ω, the output swing ranges from -3.5V to 3.5V. This response is a simple application of Ohms law indicating a lower value resistance results in greater current demands of the amplifier. Additionally, the load resistance affects the frequency response of this family as well as all operational amplifiers, as clearly indicated by the Gain vs Frequency for Various RL curves clearly indicate. In the case of the frequency response reduced bandwidth with decreasing load resistance is a function of load resistance in conjunction with the output zero response of the amplifier.

Choosing a Feedback Resistor

A feedback resistor is required to achieve unity gain; simply short the output pin to the inverting input pin. Gains greater than +1 require a feedback and gain resistor to set the desired gain. This gets interesting because the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As the feedback resistance increases the position of the pole shifts in the frequency domain, the amplifier's phase margin is reduced and the amplifier becomes less stable. Peaking in the frequency domain and ringing in the time domain are symptomatic of this shift in pole location. So we want to keep the feedback resistor as small as possible. You may want to use a large feedback resistor for some reason; in this case to compensate the shift of the pole and maintain stability a small capacitor in the few Pico farad range in parallel with the feedback resistor is recommended.

For the gains greater than unity, it has been determined a feedback resistance ranging from 500Ω to 750Ω provides optimal response.

Gain Bandwidth Product

The EL5156 and EL5157 families have a gain bandwidth product of 210MHz for a gain of +5. Bandwidth can be predicted by the following equation:

$$Gain \times BW = GainBandwidthProduct$$

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and same frequency response as DC levels are changed at the output; this characteristic is widely referred to as “diffgain-diffphase”. Many amplifiers have a difficult time with this especially while driving standard video loads of 150Ω, as the output current has a natural tendency to change with DC level. The EL5152 dG and dP for these families is a respectable 0.006% and 0.04%, while driving 150Ω at a gain of 2. Driving high impedance loads would give a similar or better dG and dP performance as the current output demands placed on the amplifier lessen with increased load.

Driving Capacitive Loads

The EL5152 and EL5153 families can easily drive capacitive loads as demanding as 27pF in parallel with 500Ω while holding peaking to within 5dB of peaking at unity gain. Of course if less peaking is desired, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with the output to eliminate most peaking. However, there will be a small sacrifice of gain which can be recovered by simply adjusting the value of the gain resistor.

Driving Cables

Both ends of all cables must always be properly terminated; double termination is absolutely necessary for reflection-free performance. Additionally, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down

The EL5152 and EL5253 can be disabled with their output placed in a high impedance state. The turn off time is about 330ns and the turn on time is about 130ns. When disabled, the amplifier's supply current is reduced to 17µA typically; essentially eliminating power consumption. The amplifier's power down is controlled by standard TTL or CMOS signal levels at the ENABLE pin. The applied logic signal is relative to V_S- pin. Letting the ENABLE pin float or the application of a signal that is less than 0.8V above V_S- enables the amplifier. The amplifier is disabled when the signal at ENABLE pin is above V_S+ -1.5V.

Output Drive Capability

The EL5152 and EL5153 families do not have internal short circuit protection circuitry. Typically, short circuit currents as high as 95mA and 70mA can be expected and naturally, if the output is shorted indefinitely the part can easily be damaged from overheating, or excessive current density may eventually compromise metal integrity. Maximum reliability is maintained if the output current is always held below ±40mA. This limit is set and limited by the design of the internal metal interconnect. Note that in transient applications, the part is extremely robust.

Power Dissipation

With the high output drive capability of the EL5152 and EL5153 families, it is possible to exceed the 125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

For sourcing:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}}$$

For sinking:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_{OUTi} - V_S) \times I_{LOADi}$$

Where:

V_S = Supply voltage

IS_{MAX} = Maximum quiescent supply current

V_{OUT} = Maximum output voltage of the application

R_{LOAD} = Load resistance tied to ground

I_{LOAD} = Load current

N = number of amplifiers (Max = 2)

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_S- pin becomes the negative supply rail. See Figure 1 for a complete tuned power supply bypass methodology.

Printed Circuit Board Layout

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

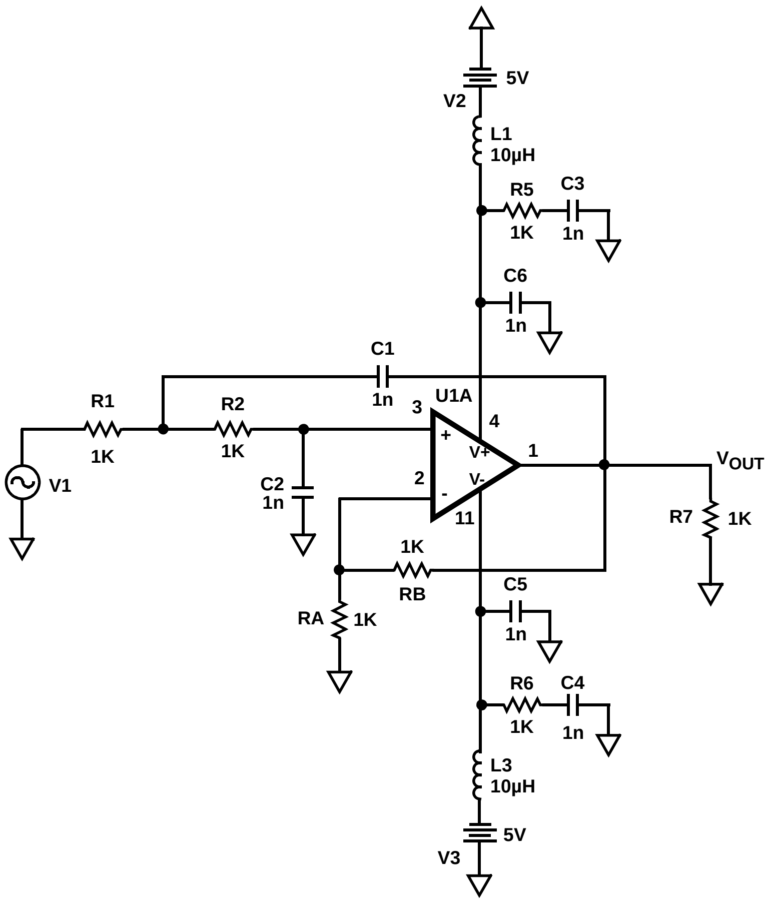
Application Circuits

Sullen Key Low Pass Filter

A common and easy to implement filter taking advantage of the wide bandwidth, low offset and low power demands of the EL5152. A derivation of the transfer function is provided for convenience. (See Figure 28.)

Sullen Key High Pass Filter

Again this useful filter benefits from the characteristics of the EL5152. The transfer function is very similar to the low pass so only the results are presented. (See Figure 29.)



$$K = 1 + \frac{RB}{RA}$$

$$Vo = K\frac{1}{R2C2s + 1}V1$$

$$\frac{V1 - Vi}{R1}1 + \frac{\frac{Vo}{K - V1}}{R2} + \frac{Vo - Vi}{\frac{1}{C1s}} = 0$$

$$H(s) = \frac{K}{R1C1R2C2s^2 + ((1 - K)R1C1 + R1C2 + R21C2)s + 1}$$

$$H(jw) = \frac{1}{1 - w^2R1C1R2C2 + jw((1 - K)R1C1 + R1C2 + R2C2)}$$

$$Holp = K$$

$$wo = \frac{1}{\sqrt{R1C1R2C2}}$$

$$Q = \frac{1}{(1 - K)\sqrt{\frac{R1C1}{R2C2}} + \sqrt{\frac{R1C2}{R2C1}} + \sqrt{\frac{R2C2}{R1C1}}}$$

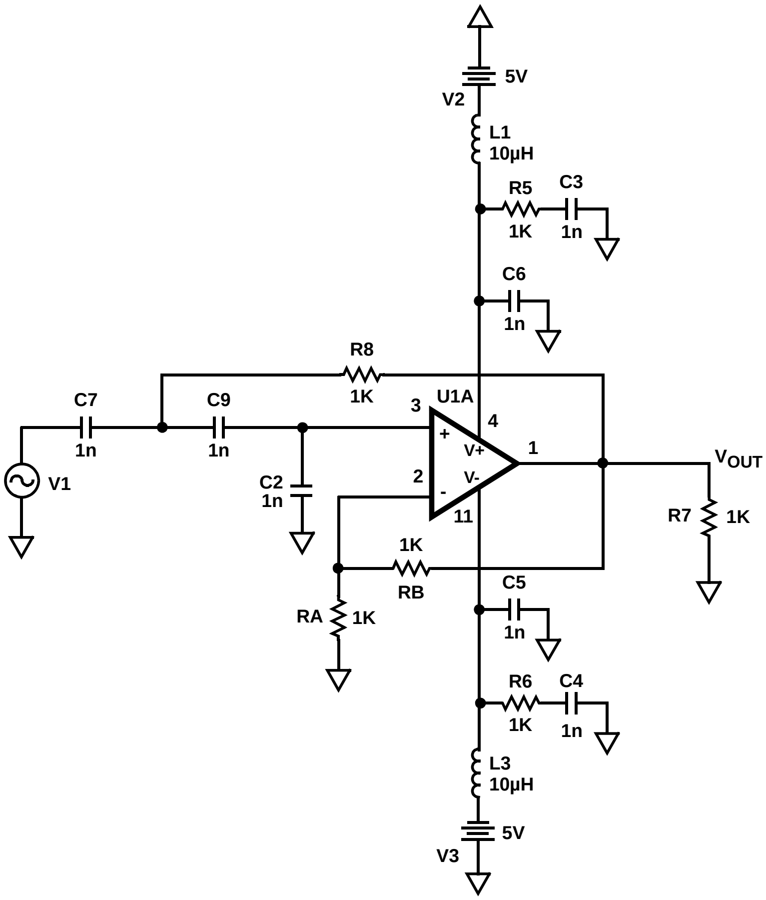
$$Holp = K$$

$$wo = \frac{1}{RC}$$

$$Q = \frac{1}{3 - K}$$

Equations simplify if we let all components be equal R=C

FIGURE 28. SULLEN KEY LOW PASS FILTER



$$Holp = K$$

$$wo = \frac{1}{\sqrt{R1C1R2C2}}$$

$$Q = \frac{1}{(1-K)\sqrt{\frac{R1C1}{R2C2}} + \sqrt{\frac{R1C2}{R2C1}} + \sqrt{\frac{R2C2}{R1C1}}}$$

$$Holp = \frac{K}{4-K}$$

$$wo = \frac{\sqrt{2}}{RC}$$

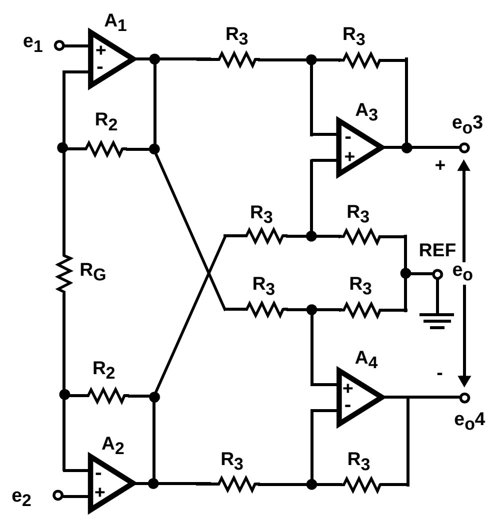
$$Q = \frac{\sqrt{2}}{4-K}$$

Equations simplify if we let all components be equal R=C

FIGURE 29. SULLEN KEY HIGH PASS FILTER

Differential Output Instrumentation Amplifier

The addition of a third amplifier to the conventional three amplifier Instrumentation Amplifier introduces the benefits of differential signal realization, specifically the advantage of using common mode rejection to remove coupled noise and ground-potential errors inherent in remote transmission. This configuration also provides enhanced bandwidth, wider output swing and faster slew rate than conventional three amplifier solutions with only the cost of an additional amplifier and few resistors.



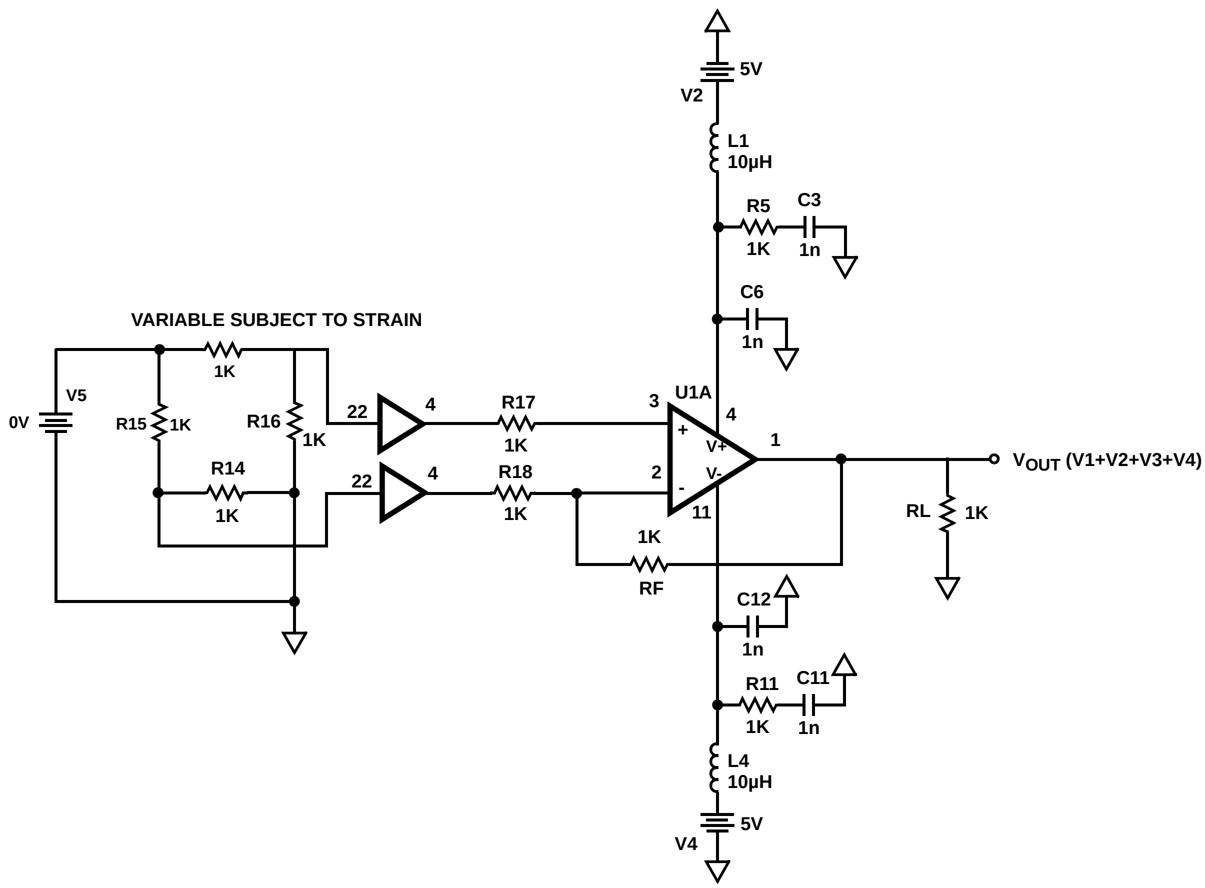
$$e_{o3} = -(1 + 2R_2/R_G)(e_1 - e_2) \qquad e_{o4} = (1 + 2R_2/R_G)(e_1 - e_2)$$

$$e_o = -2(1 + 2R_2/R_G)(e_1 - e_2)$$

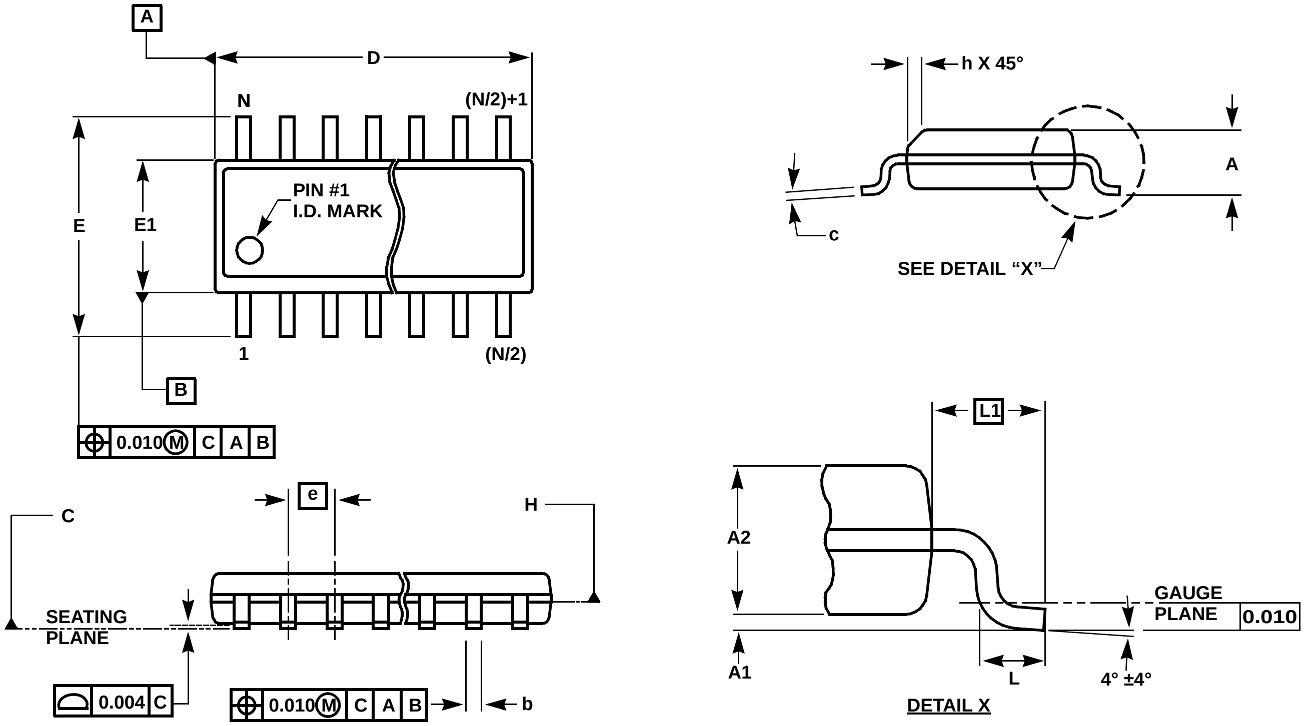
$$BW = \frac{2f_{C1,2}}{|A_{Di}|} \qquad A_{Di} = -2(1 + 2R_2/R_G)$$

Strain Gauge

The strain gauge is an ideal application to take advantage of the moderate bandwidth and high accuracy of the EL5152. The operation of the circuit is very straight forward. As the strain variable component resistor in the balanced bridge is subjected to increasing strain its resistance changes resulting in an imbalance in the bridge. A voltage variation from the referenced high accuracy source is generated and translated to the difference amplifier through the buffer stage. This voltage difference as a function of the strain is converted into an output voltage.



Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

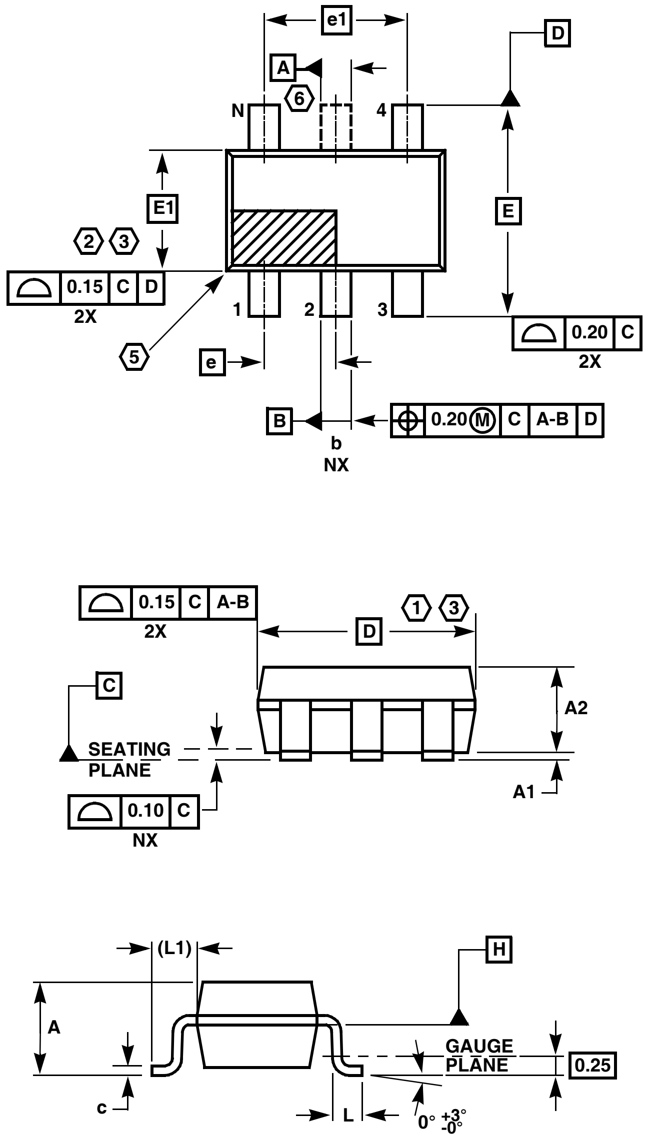
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

SOT-23 Package Family



MDP0038

SOT-23 PACKAGE FAMILY

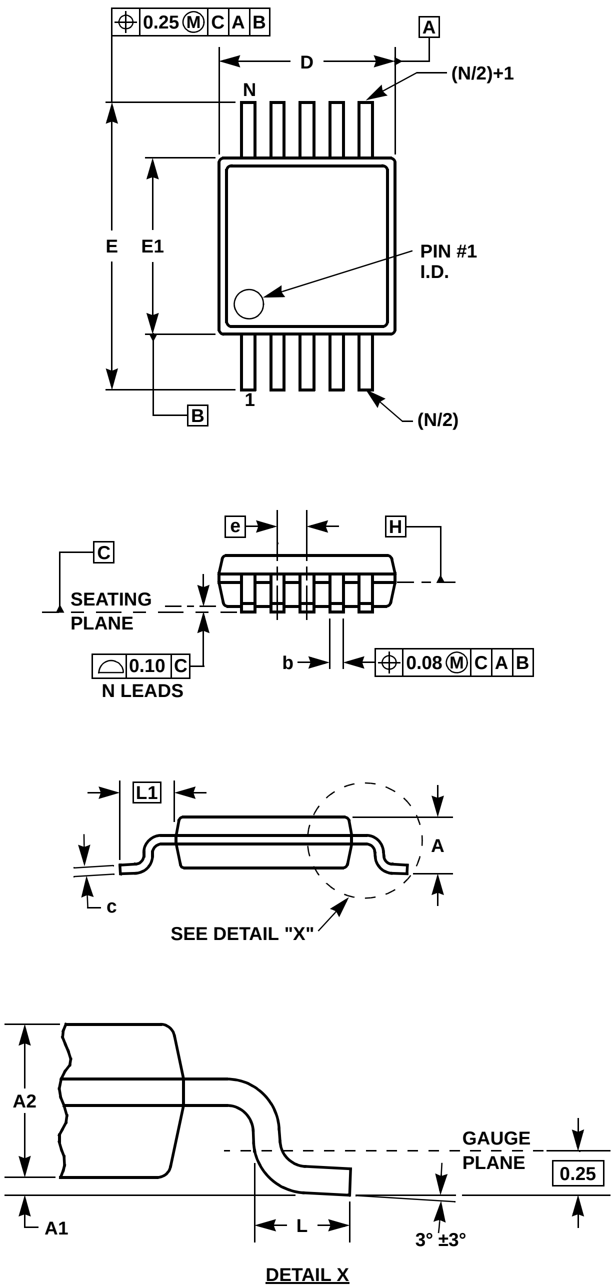
SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.